

REMARKS

Claims 29 to 36, while withdrawn, are retained and listed as previously presented since they represent interfering subject matter and should be handled in this application on a special basis since they relate to interfering subject matter for reasons stated in the Petition, previously filed, a copy of which is attached hereto. The subject matter of the Petition is incorporated herein by reference.

Claims 21, 22, 24, 25 and 28 were rejected under 35 U.S.C. 102(b) as being anticipated by Cotues et al. (U.S. 5,239,447). The rejection is again respectfully traversed.

Claim 21, from which claims 22, 24, and 28 depend require, among other features, “electrically connecting said at least one electrical terminal on said at least one edge surface of said integrated circuit package to said top surface of said printed circuit board at an acute angle with said top surface of said printed circuit board”. No such feature is taught or even remotely suggested by Cotues et al. Note with respect to figures 4 and 5 of Cotues et al. that the terminal is not on the edge surface of the package but rather on a major surface. The surface 76 of Cotues et al. is specifically stated at column 5, lines 47ff to be “a dielectric layer such as a silicon dioxide layer or other dielectric coating on a silicon electronic device 40”. It follows that the edge surface of the integrated circuit package of Cotues et al. is not an electrical terminal as required by claim 21 and is not electrically connected to the circuit board.

Claims 22 to 25, 27 and 28 depend from claim 21 and therefore define patentably over Cotues et al. for at least the reasons set forth above with reference to claim 21.

In addition, claim 22 further limits claim 21 by requiring the step of electrically and perpendicularly connecting at least two integrated circuit packages to the circuit board. No such combination is taught or suggested by Cotues et al..

[Claim 23 further limits claim 21 by requiring the step of disposing a solder ball between the side surface terminal of the integrated circuit package and the top of the circuit board. No such combination is taught or suggested by Cotues et al.]

Claim 25 further limits claim 21 by requiring the step of integrally attaching at least three tabs to said circuit board. No such combination is taught or suggested by Cotues et al.

Claim 28 further limits claim 21 by requiring that the at least one edge surface is four edge surfaces, each of the four edge surfaces disposed between the major surfaces to form a closed package with the major surfaces. No such combination is taught or suggested by Cotues et al.

Claims 27 and 38 were rejected under 35 U.S.C. 103(a) as being unpatentable over Cotues et al. The rejection is respectfully traversed.

Claim 27 further limits claim 21 by requiring that the integrated circuit package be further defined as being connected at an acute angle between 30 and less than 90 degrees to the circuit board. No such feature is is taught or suggested by Cotues et al. either alone or in the combination as claimed.

Claim 38 is patterned after claim 27 and defines patentably over Cotues et al. for the reasons presented above with reference to claim 27.

Claims 21 to 25, 27, 28 and 38 were rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki et al. (U.S. 5,726,492) in combination with Fujisawa et al. (U.S. 6,094,356). The rejection is respectfully traversed.

All of the rejected claims other than claims 21 and 38 depend from claim 21. Accordingly, the argument presented hereinbelow applies to all of the rejected claims.

It is readily apparent that Suzuki et al. teach mounting semiconductor chips 22 onto a substrate 24 with wiring pattern thereon 24a via solder bumps 23a. It is not the chip 22, but rather the substrate 24 via the wiring pattern 24a thereon which is connected to the main substrate 32. This has nothing whatsoever to do with the claimed invention herein. It therefore follows that, even were Fujisawa et al. to teach that which is alleged, there would still be no basis for the combination. However, a review of Fujisawa et al. will indicate that the terminal 16A is not connected to the edge surface of the chip 12, but rather travels over a major surface thereof where the connection is made. It follows that the terms of the rejected claims are not met by either reference or any combination thereof, proper or improper.

In view of the above remarks, favorable reconsideration and declaration of an interference and/or interferences as indicated above are respectfully requested.

Respectfully submitted,



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